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IN RE U.S. PATENT APPLICATION
APPLICATION NUMBER: 10/665,757
FILED: 9/19/2003 CONFIRMATION NO. 6828

TRANSMITTAL COVER LETTER FOR FACSIMILE TRANSMISSION

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ELM-1 Cont. 9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Glenn J. Leedy
Application No. : 10/665,757 Confirmation No. : 6828
Filed : September 19, 2003
For : METHOD OF MAKING AN INTEGRATED CIRCUIT
Examiner : Pamela E. Perkins
Art Unit : 2822

New York, New York 10020
April 26, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicant wishes to call the attention of the Examiner to the
following documents:

U.S. Patent Documents

Groschwitz	01-18-1972	US 3,636,358
Takatsu et al.	01-21-1986	US 4,566,037
Tanimoto et al.	11-11-1986	US 4,622,632
Furtek et al.	09-14-1993	US 5,245,227
Bayer et al.	02-01-1994	US 5,283,107
Arima et al.	03-08-1994	US 5,293,457
Dasse et al.	03-21-1995	US 5,399,505
Davies	09-12-1995	US 5,450,603
Gallup et al.	11-05-1996	US 5,572,689

04/27/2006 SSITHIB1 00000100 061075 10665757
01 FC:1806 180.00 DA

U.S. Patent Documents

Roussakov	07-18-2000	US 6,092,174
Ikenaga et al.	11-28-2000	US 6,154,809
Sobel et al.	10-09-2001	US 6,300,935
Mohamed et al.	10-09-2001	US 6,301,653
Sobel et al.	11-20-2001	US 6,320,593
Leedy	02-03-2005	US 2005/0023656
Gudesen et al.	05-17-2005	US 6,894,392

Nonpatent Literature Document

WOLF, S. et al., "SILICON PROCESSING FOR THE VLSI ERA," Process Technology, Latice Press, Sunset Beach, CA, Vol. 1, pp. 191-194, 1986.

The aforementioned references are listed on the accompanying Form PTO/SB/08 (submitted in duplicate). Pursuant to 37 C.F.R. § 1.98(a)(2), no copies of the aforementioned U.S. Patent Documents are being submitted. A copy of the Nonpatent Literature Document is being submitted herewith.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

It is respectfully requested that these references be: (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO/SB/08, as considered and

initialled by the Examiner, be returned with the next communication.


The documents cited above were cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/741,647 on January 26, 2006.

Pursuant to 37 C.F.R. § 1.97(e), applicant hereby certifies that the documents listed above were not cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, were known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Supplemental Information Disclosure Statement.

The Director is hereby authorized to charge \$180.00 in payment of the fee for submission of this Supplemental Information Disclosure Statement pursuant to 37 C.F.R. § 1.97(d)(2), payment of any additional fees required in connection with this Statement, or credit any overpayment of the same, to Deposit Account No. 06-1075, Order No.: 001202.0001. A duplicate copy of this Supplemental Information Disclosure Statement is enclosed herewith.

An early and favorable action is respectfully
requested.

Respectfully submitted,



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Substitute for form 1449A/B/PTO				Complete if Known	
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/665,757 (Conf. No. 6828)
				Filing Date	September 19, 2003
				First Named Inventor	Glenn J. Leedy
				Art Unit	2822
				Examiner Name	Pamela E. Perkins
Sheet	1	of	1	Attorney Docket Number	ELM-1 Cont.9

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US 3,636,358	01-18-1972	Groschwitz	
		US 4,566,037	01-21-1986	Takatsu et al.	
		US 4,622,632	11-11-1986	Tanimoto et al.	
		US 5,245,227	09-14-1993	Furtek et al.	
		US 5,283,107	02-01-1994	Bayer et al.	
		US 5,293,457	03-08-1994	Arima et al.	
		US 5,399,505	03-21-1995	Dasse et al.	
		US 5,450,603	09-12-1995	Davies	
		US 5,572,689	11-05-1996	Gallup et al.	
		US 6,092,174	07-18-2000	Roussakov	
		US 6,154,809	11-28-2000	Ikenaga et al.	
		US 6,300,935	10-09-2001	Sobel et al.	
		US 6,301,653	10-09-2001	Mohamed et al.	
		US 6,320,593	11-20-2001	Sobel et al.	
		US 2005/0023658	02-03-2005	Leedy	
		US 6,894,392	05-17-2005	Gudesen et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		Country Code ³ -Number ⁴ -Kind Code ⁵ (If known)				

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		WOLF, S. et al., "SILICON PROCESSING FOR THE VLSI ERA," Process Technology, Lattice Press, Sunset Beach, CA, Vol. 1, pp. 191-194, 1986.	

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		Filing Date	September 19, 2003
		First Named Inventor	Glenn J. Leedy
		Art Unit	2822
		Examiner Name	Pamela E. Perkins
		Attorney Docket Number	ELM-1 Cont.9
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		US 6,154,809	11-28-2000	Ikenaga et al.	
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		US 2005/0023656	02-03-2005	Leedy	
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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS				
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		WOLF, S. et al., "SILICON PROCESSING FOR THE VLSI ERA," Process Technology, Lattice Press, Sunset Beach, CA, Vol. 1, pp. 191-194, 1986.		

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